A Novel Low-Energy CNTFET-Based Ternary Full-Adder Design using Unary Operators

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***Abstract*—In the present world the consumption of energy is a critical factor. The energy consumption has to be reduced for designing the embedded systems .Through Multiple-valued logic (MVL) circuits, interconnections complexity and energy consumption their is decrease in comparison to binary systems. In this paper we used MVL circuits to present a ternary full-adder (TFA) which reduces the consumption of the energy for the maintenance of the battery in nano-scale embedded systems and IoT devices. In this paper we used CNTFET-based circuit which uses a dual- voltage (Vdd and Vdd/2) and novel unary operators to improve the performance of the designed system.**

***Index Terms*—Carbon Nano-Tube Field Effect Transistors (CNTFET), Multiple-Valued Logic (MVL),Ternary logic circuits, Unary Operators.**

1. INTRODUCTION

**T**

HE nano-scale embedded systems and IoT devices faces two major problems: the Complementary Metal Oxide Semiconductor (CMOS) transistor technology and bi-

nary circuits.

The first issue in the embedded systems and IoT devices is the CMOS transistor technology which has complications such as high current leakage, close channel effects, loss of gate power, etc. [1]. Researchers have provided many solutions to these problems, such as Fin Field Effect Transistor (FinFET), Single-Electron Systems, Spin-wave, CNTFET, and others. The most effective one among them is the CNTFET which has the highest performance [2].

The second issue is that the binary circuits requires lot of interconnections and high energy consumption. Using Multiple-Valued Logic (MVL) circuits, interconnections and energy consumption are reduced.

Recently, MVL has been the most interesting topic for scientists, they implemented it in different applications such as the Analog Circuit [3], Machine learning & IoT [4], Healthcare [5], Algorithm [6],

1. , and ternary circuits like Ternary Decoder [8], Memory [9], [10], Binary to Ternary converter [11], and Memristor [12].

While compared to other base systems, the ternary system has the lowest circuit cost and complexity [13]. There are two ways for implementation of the ternary system : Balanced (-1, 0, 1) equivalent to (-Vdd, 0, Vdd) and Unbalanced (0, 1, 2) equivalent to (0, Vdd/2, Vdd).In this paper we have used the unbalanced method of ternary system.

In order to get the logical state 1 (Vdd/2) in a ternary circuit using a single power supply (Vdd) is quite a bit challenging. So the researchers inserted two resistors that work as a voltage divider to produce the ternary logical state 1 (Vdd/2) but it is not suitable in VLSI circuits because it cause increase in the circuit size. For better approach we can use diode-connected transistors that act as resistors, but this lead to the significant increase in static power dissipation caused due to the direct current passing from the power supply (Vdd) to the ground [14]. To eliminate the direct current path, we used dual voltage(Vdd and Vdd/2) in this paper .

Through, this paper we proposes a CNTFET-based design for a low-energy TFA using novel unary operators of ternary logic (small circuits used to implement any ternary circuit and could replace the basic logic gates, see Section IV) and dual-voltage (Vdd, Vdd/2) techniques to preserve the battery consumption of embedded systems and IoT devices.

The rest of the paper is organized as follows: Section II contains a literature review. Section III provides a background for the CNTFET Model. Section IV proposes novel designs for unary operators. Section V presents the ternary half adder. Section VI shows simulation results and comparisons. Section VII concludes the presented work.

1. LITERATURE REVIEW

Many publications used CNTFET to implement THAs, as well as TFA the important and latest ones are summarized below.

Authors of [15]–[17] used ternary decoders (TDecoders), binary logic gates, ternary encoders, and ternary logic gates to design THAs with 136, 112, and 112 CNTFETs, respectively.

In research paper[18], they proposed a TDecoder with 9 CNTFETs, a Ternary NAND, a Standard Ternary Inverter (STI), and used a dual-voltage (Vdd and Vdd/2) to implement a THA with 85 CNTFETs.

In [19], the authors designed a THA with 168 CNTFETs using cascading TDecoder-based (3:1) ternary multiplexers (TMUXs) with 28 CNTFETs.

The authors of [14], [21]–[24] proposed THAs with 39,

64, 54, 76, and 48 CNTFETs, respectively using different unary operators and TMUX designs. In [21] and [22], the authors designed ”decoder-less” (3:1) TMUXs with 15 & 18 CNTFETs, and designed high energy consumption unary operators using a single power supply (Vdd), which has a direct current path from the power supply to the ground .

III. CNTFET MODEL

A carbon nanotube field-effect transistor (CNTFET**)** is a field-effect transistor which has a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk  silicon  in the traditional MOSFET structure.

In Stanford CNTFET model [32] the channel that being used is a semiconducting single-walled CNT conduction channel, which gives better performance when compared with the other types of transistors i.e., MOSFET and CMOS, even with device non idealities. Figure 1 shows the Stanford CNTFET model as described in [32].

The properties of CNTFET model are pretty much similar as that of the MOSFETs, with an exception of threshold voltage which depends on the diameter of the CNT, as stated in equation (1)

*V*th

= *√*3 *c · V π*

3 *e · Dcnt*

(1)

Authors of [22] proposed THAs with CNTFETs using an unary operators for logic synthesis. And for TFA they used MUX for the design. These MUX they have used are formed from the equations that are reduced using the unary operators.

But, the previously used designs have issues such as high number of transistors, high energy consumption, low process variation robustness, or low noise tolerance.

*A. Contributions*

In this work, we propose a TFA with CNTFETs using novel unary operators and a dual-voltage (Vdd, Vdd/2) to achieve the lowest Power-Delay Product (PDP) and preserve battery consumption in nano-scale embedded systems and IoT devices.

The contributions in our designs are summarized and stated as follows:

* 1. The proposed TFA uses novel unary operators of the ternary system instead of using basic logic gates, Tdecoders, or TMUXs, which reduces transistors count and energy consumption.
  2. The proposed unary operators use a dual-voltage (Vdd and Vdd/2) technique to remove the direct current path from Vdd to the ground, which also results in lower energy consumption .

Where *V π* = 3.033 eV represents the carbon bond energy, *c* = 2.49 A˚ is the atom distance from carbon-to-carbon, *e* is the electron charge unit, and *Dcnt* represents the diameter of CNT.

From Table I we can get the relationship between the diameter, threshold voltage, and the operation of the CNTFET transistor .

1. PROPOSED UNARY OPERATORS

Unary functions (operators) of *b*-valued logic system are one-input/one-output logic gates with a total number of func- tions equal to *bb*, as defined in [33].

If we use binary system then (*b*=2), then their existsfour (22) unary functions (00, 01, 10, 11). Where as in ternary system (*b*=3),

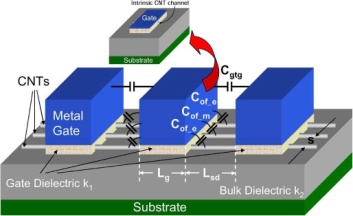


Fig. 1: Stanford CNTFET Model in [32].

TABLE I: CNTFET Operation with D1= 1.487 nm and D2= 0.783 nm

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Type | Diameter | Threshold  voltage | Voltage Gate  0V 0.45V 0.9V | | |
| P-CNTFET | D1 | - 0.289 V | ON | ON | OFF |
|  | D2 | - 0.559 V | ON | OFF | OFF |
| N-CNTFET | D1 | 0.289 V | OFF | ON | ON |
|  | D2 | 0.559 V | OFF | OFF | ON |

TABLE II: Truth Table of the Three Ternary Inverters

|  |  |  |  |
| --- | --- | --- | --- |
| Ternary Input  *A* | STI  *A*¯ | PTI  *Ap* | NTI  *An* |
| Logic 0 (0V) | 2 | 2 | 2 |
| Logic 1 (0.45V) | 1 | 2 | 0 |
| Logic 2 (0.9V) | 0 | 0 | 0 |

TABLE III: Proposed Four Unary Operators

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Ternary  Input *A* | 1 |  | *A*¯*n* | 1 | *· A*¯*p* | Cycle  *A*1 | Operators  *A*2 |
| 0 (0V) | 0 | | | 0 | | 1 | 2 |
| 1 (0.45V) | 1 | | | 0 | | 2 | 0 |
| 2 (0.9V) | 1 | | | 1 | | 0 | 1 |

**Vdd/2**



**T1**

**D1**

**An**

**T2 D2**

# (a)

1. **An**

**Vdd**

**Vdd/2**

TABLE IV: Proposed Unary Operators Operation

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Fig. 2 | *A* | *An* | *Ap* | Transistors Status  ON OFF | | Output | | |
|  | 0 | 2 |  | T2 | T1 | 0 | ) | **1** *·* **An** |
| (a) | 1  2 | 0  0 |  | T1  T1 | T2  T2 | 1  1 |
|  | 0 |  | 2 | T2 | T1 | 0 | ) | **1** *·* **Ap** |
| (b) | 1  2 |  | 2  0 | T2  T1 | T1  T2 | 0  1 |
| (c) | 0  1  2 | 2  0  0 |  | T2,T4  T1,T2 T1,T3 | T1,T3  T3,T4 T2,T4 | 1  2  0 | ) | **A1** |
| (d) | 0  1  2 |  | 2  2  0 | T1  T2 T3 | T2,T3  T1,T3 T1,T2 | 2  0  1 | ) | **A2** |

**Vdd/2**

**T1**



**An**

**T1 T4 D1 D2**

**A**

**A**

**T2 D1**

**A1**

**T3 D2**

**(c)**

**D1**

**Ap 1.Ap**

**T2 D2**

# (b)

**Vdd**

**A**



**T1 T3**

**D2 D1**

**Ap**

**A**2

**T2 D2**

**A1**

**Vdd/2**

# (d)

there will be twenty-seven (33) unary operators (000, 001, 002,..., 220, 221, 222).

From Table II the truth table of 3 ternary inverters, which are also unary operators of ternary logic is explained:**D1=1.487nm |Vth|= 0.289V; D2=0.783nm |Vth|= 0.559V**

Fig. 2: Proposed Four Unary Operators: (a) 1 *A*¯*n*, (b) 1 *A*¯*p*,

*· ·*

* 1. *A*1, and (d) *A*2.

TABLE V: Comparison of Unary Operators Transistors Count

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **[14]** | **[22]** | **[23]** | **[24]** | Proposed | Improvement  w.r.t [22] |
| **1** *·* **A¯p**  **1** *·* **A¯n A1**  **A2** | -  - 17  17 | 5  5  7  7 | 4  4  10  10 | 10  10  18  18 | 2  2  4  3 | 60%  60%  42.86%  57.14% |

A¯ (Standard Ternary Inverter (STI)), Ap (Positive Ternary

Inverter (PTI)), and *An* (Negative Ternary Inverter (NTI)).

In this paper we have used four novel unary operator’s designs (1 A¯n, 1 A¯p, A1, and A2), that are shown in Table III and represented in Fig 2. The first and second unary operators work as two- inputs TANDs 1 A¯n and 1 A¯p. The third and fourth unary operators are named cycle operators, A1 is A + 1 and A2 is A + 2.

*· ·*

*· ·*

The proposed unary operators’ operations are displayed in Table IV, and the comparison of their number of transistors is presented in Table V.

The Sum and the Carry equations of full adder using

the truth table which is presented in the Table V and we

also used the unary operators that are mentioned above in

the Table III :

1. PROPOSED TERNARY Full-ADDER

A 1-trit TFA is a circuit that adds three ternary inputs (*A,B* and C) and produces two outputs: the Sum and the Carry, as illustrated in Table VI.

In this paper, we proposed a TFA using unary functions.Sum = c0 [b0 · A + b1 · A1 + b2 · A2]

+ c1 [b0 · A1 + b1 · A2 + b2 · A]

+ c2 [b0 · A2 + b1 · A+ b2 · A1]

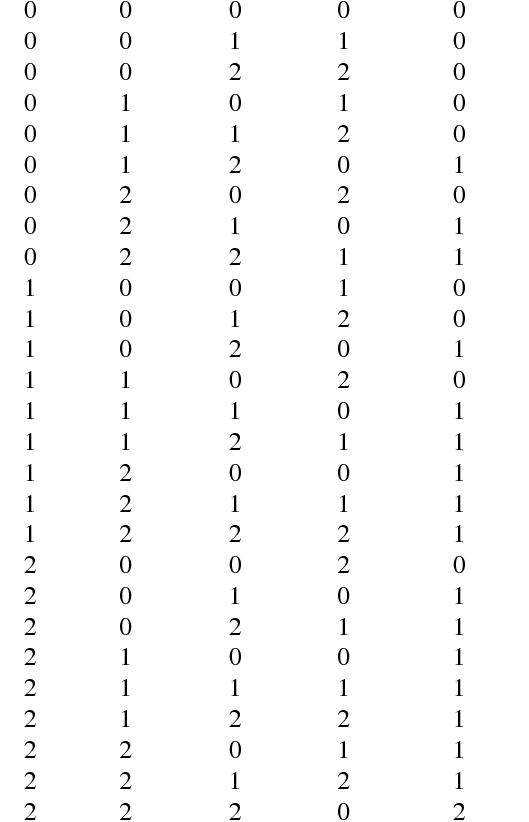
Carry = c0 [b0. 0 +b1. (1 . Ap) + b2. (1.An)]

+ c1 [b0. (1 . Ap) +b1. (1 . An) + b2 .1]

+ c2 [b0 . (1 . An) +b1 .1 + b2 . (1 +. Ap)]

Table VI : Truth Table of TFA

A B C SUM CARRY



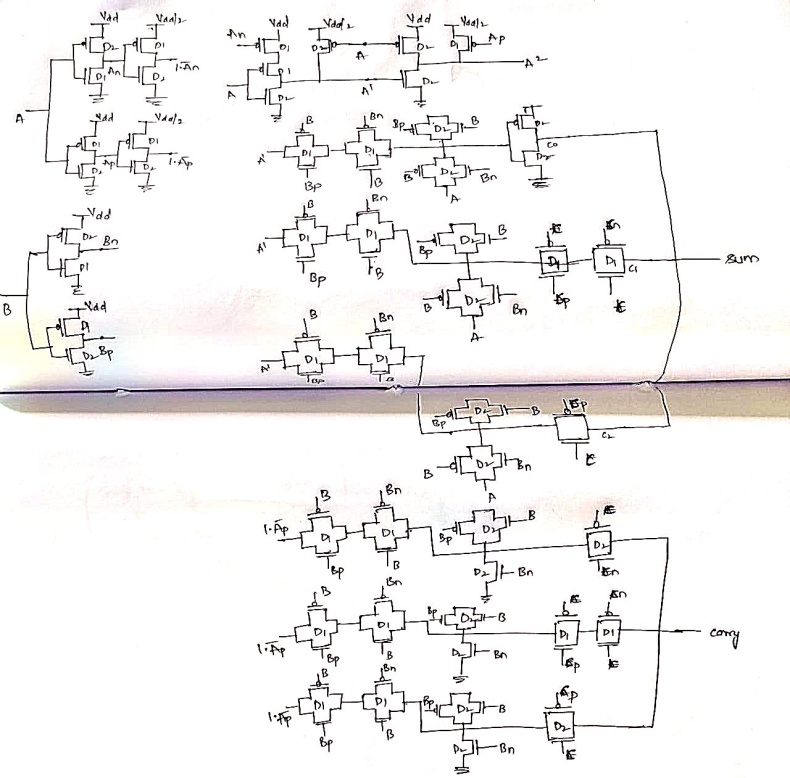


Fig 3: proposed TFA with CNTFET’s using unary operators.

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